(12) EUROPEAN PATENT APPLICATION

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(54) Variable gain amplifier for low supply voltage.

(57) A variable gain amplifier is composed of a first voltage-to-current amplifier having a fixed gain; a second voltage-to-current amplifier having a variable gain, functioning in parallel to said first amplifier; a gain control and stabilization variable current generator; a current-to-voltage converter. Current output signals produced by said first and second amplifiers and by said variable current generator are summed and the resulting current signal is converted to a voltage signal by said converter.
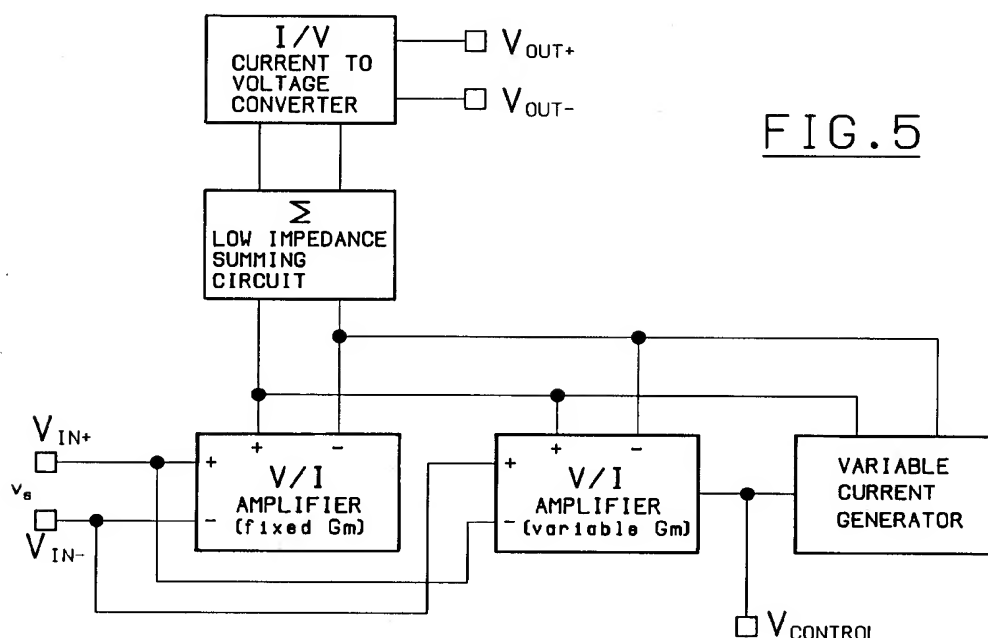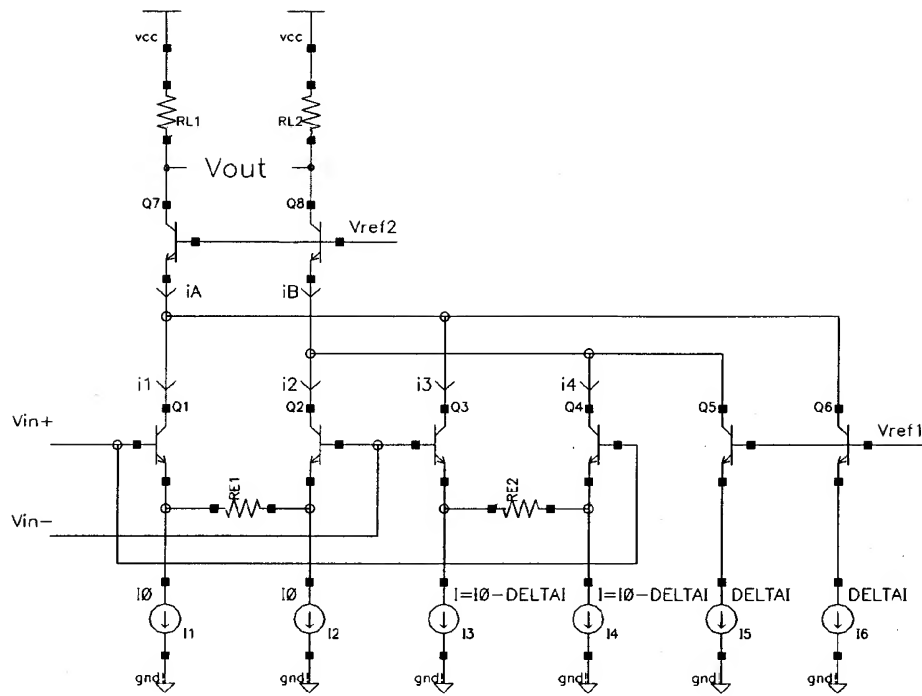
FIG.5

F I G . 6

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The present invention relates to a variable gain amplifier (VGA) particularly suited for automatic gain control systems (AGC).

Typically, automatic gain control (AGC) systems are implemented by employing a variable gain amplifier (VGA) , a detector (a peak or average value detector) capable of providing an information on the signal level in the loop, and a bidirectional current generator driven by the detector and finally a capacitor for stabilizing the loop and constituting an analog memory of the system. A system of this type is schematically shown in Fig. 1.

Characterizing performance parameters of a variable gain amplifier (VGA) , may be listed as follows:
* Frequency band
* Range of variation of the gain
* Maximum level of the input signal
* Maximum level of the output signal
* Linearity
* Output offset
* Equivalent input noise

Specific requirements dictated by the particular field of application and therefore different performance parameters determine the choice among numerous amplifier circuits, suitable to be integrated on silicon.

In order to implement an automatic gain control before a demodulation stage of the Intermediate Frequency block of a TV receiver, it is necessary to provide for an interval of variation of the gain of about 60dB. Therefore, it is often necessary to employ a chain of several amplifying stages in cascade. On ther other hand, in consideration of the band characteristics of the processed TV signal, the coupling between the various stages is usually implemented in an AC mode. Therefore, the output offset that was mentioned above among other merit parameters of a VGA, loses its relevance in this case. A typical amplifier structure that is employed in integrated TV circuits for implementing a VGA is shown in Fig. 2.

If the control current: Icont = 0, the gain of the stage is almost equal to the ratio 2RL/RE, where RE is the total emitter-degeneration resistance. By increasing Icont, the diodes turn on and, by adding their own impedance: 1/gm, in parallel to the modules that make up RE, modify (decrease) the gain.

Conversely, in the case of an automatic gain control implementation in a read/write channel of a hard disk, a typical set of performance parameters of a variable gain amplifier suited for this type of application may be indicated as follows:
* Frequency band: from 0 to 30 MHz
* Gain variation: from 4 to 80 Volt/Volt (26dB)
* Input signal: from 12mVpp to 250mVpp (differential)
* Output signal: from 1.0Vpp to 3Vpp (differential)
* Linearity: better than 40dB (Distorsion <1%)
* Output offset: less than +/- 400mV
* Equivalent input noise: < 15nV/sqrt(Hz)
* Supply voltage: from 4.5V to 5.5V

In view of the relatively limited variation of the gain that is required (26dB), a typical VGA structure that is customarily used for such an application, is constituted by a single variable gain stage "cell", followed by a fixed gain stage, typically having a gain of 10/20Volt/Volt.

A variable gain stage that is commonly used in these applications is shown in Fig. 3. It utilizes a common circuit known as "double Gilbert multiplier circuit", which permits to vary in a continuous fashion the gain by controlling the balance in the upper quadrants and by approximately maintaining constant the DC operating point throughout the range of gain variation.

Such a known circuit has the advantage of neutralizing the Miller effect of multiplication of a parasitic base/collector capacitance, representing in practice a cascode (grounded-base) configuration. This permits to achieve a broad band characteristic.

The integration of a read/write "channel" in a single chip and the increase of the data transfer speed have made even more stringent the requirements for the VGA to be employed, as may be set forth by the following values of required performance parameters:
* Frequency band: from 0 to 50 MHz
* Gain variation: from 2 to 22 Volt/Volt (21dB)
* Input signal: from 20mVpp to 240mVpp (differential)
* Output signal: maximum 1.1Vpp (differential)
* Linearity: better than 40dB (Distorsion <1%)
* Output offset: less than +/- 200mV
* Equivalent input noise: < 15nV/sqrt(Hz)

* Supply voltage: from 4.3V to 5.5V

The broadening of the frequency band that is required because of an increased data transfer speed, has made necessary the use of a further cascode stage for further decreasing the parasitic capacitance of the gain control resistance, according to the diagram shown in Fig. 4.

More recent developments of hard disk memory systems have imposed a further mark-up of the design parameters of the AGV to be used in these state of the art systems.

Nowadays, hard disk memories are no longer exclusively installed in fixed installations, but ever more often they are installed in portable (battery operated) instruments and the power consumption has assumed a critical importance. Moreover, these modern systems tend to be faster and faster.

As a consequence, read/write systems must be compatible with a relatively low supply voltage of about 3Volt, the required frequency band may be up to about 80MHz because of increase speed while the other parameters may remain practically unchanged. A sample specification of an AGV for this type of applications, characterized by a relatively low supply voltage, may be as follows:

* Frequency band: from 0 to 80 MHz
* Gain variation: from 2.7 to 33 Volt/Volt (22dB)
* Input signal: from 20mVpp to 240mVpp (differential)
* Output signal: maximum 0.75Vpp (differential)
* Linearity: better than 40dB (Distorsion <1%)
* Output offset: less than +/- 200mV
* Equivalent input noise: < 15nV/sqrt(Hz)
* Supply voltage: from 3V to 5.5V

AGV circuits that have been employed so far, fall short of reaching these performances. By considering for example the circuit of Fig. 4, it is evident that it is unable to provide a sufficiently wide dynamic range, capable of ensuring a correct operation with a 3Volt supply.

The main aim of the present invention is to provide a variable gain amplifier (AGV) having particularly high dynamic characteristics and a broad frequency band though working with a relatively low supply voltage.

It has now been found and represents an object of the present invention a variable gain amplifier circuit capable of satisfying such a primary requirement of a large output dynamic characteristic even under relatively low supply voltage and a broad frequency band that makes it particularly suited for battery operated portable hard disk memory systems.

Basically, the variable gain amplifier of the invention is composed of a first voltage-to-current, fixed gain amplifier and of a voltage-to-current, variable gain amplifier that operates in parallel with the first amplifier. A variable current generator permits to stabilize the DC operating point of the amplifier while varying the gain.

In practice, the current output of the three component blocks is summed before being converted back to a voltage signal by a current-to-voltage converter.

The converter may be functioanlly constituted by two load elements, for example by two load resistances, through which the sum current flows.

According to a preferred embodiment of the invention, the sum of the output current signals of the three circuit blocks may be performed by employing a summing circuit. A suitable summing circuit may be conveniently made of a transistor connected in a cascode configuration (i.e. a grounded-base configuration), so that an emitter node of the transistor may provide a desired low impedance node onto which the three different current signals may be summed. Of course, this summing circuit is not strictly necessary and under particular conditions may also be omitted, without jeopardizing the functioning of the AGV.

The invention will now be described by referring to the attached drawings which show an important embodiment of the invention which is herein incorporated by express reference.

Figure 1 shows a functional block diagram of an automatic gain control system employing a variable gain amplifier (AGV), as already mentioned above.

Figure 2 shows a circuit diagram of a variable gain "cell" (or stage) that is commonly used for realizing an AGV, as already mentioned above.

Figure 3 shows a variable gain "cell" employing a double Gilbert multiplier, according to another known solution, as already described above.

Figure 4 shows a circuit similar to that of Fig. 3, wherein a cascode stage is added in order to decrease the parasitic capacitance of the gain control resistance, as already described above.

Figure 5 is a block diagram of an AGV made according to the present invention.

Figure 6 is a simplified circuit diagram of a variable gain amplifier of the invention.

The improved structure of AGV amplifier object of the invention is shown in the form of a block diagram in Fig. 5. The AGV structure comprises a first voltage-to-current (V/I) amplifier having a fixed gain (fixed

Gm) and a second voltage-to-current (V/I) amplifier having a variable gain (variable Gm) which operates in parallel with the first amplifier. The output currents of the first amplifier and of the second amplifier are summed together and with a third current signal that is generated by a variable current generator (VARIABLE CURRENT GENERATOR) which is driven by a control voltage: ($V_{CONTROL}$).

Preferably, as already mentioned before and schematically shown in Fig. 5, a summing circuit (Σ) may be used between the outputs of the three circuit blocks and a current-to-voltage converter (I/V) , in order to provide a low impedance node onto which performing the sum of the output currents.

Therefore, a current-to-voltage (I/V) converter converts into a voltage signal the resulting sum of the output current signals of the three blocks.

A preferred embodiment of the invention is depicted in Fig. 6.

By referring to Fig. 6, a first voltage-to-current amplifier having a fixed gain is constituted by the differential pair of transistors Q1 and Q2, that is emitter-degenerated by the resistance RE1. A fixed biasing current IØ is forced through the differential pair by a pair of constant current generators I1 and I2.

The diffential pair of transistors Q3 and Q4, emitter-degenerated by the resistance RE2, constitutes a second voltage-to-current amplifier that operates in parallel with the first amplifier composed of the pair Q1 and Q2. The second amplifier operating in parallel with the first, has a variable gain. The variation of the gain of the second amplifier takes place by subtracting to a biasing current IØ that is generated by two respective current generators I3 and I4, a certain variable current: DELTAI. A generator of a variable current DELTAI is composed of the pair of transistors Q5 and Q6 that are controlled by the voltage Vref1, and of the current generators I5 and I6.

The pair of transistors Q7 and Q8, in a grounded-base configuration (cascode), has a double function. A first function is that of providing a low impedance node, such as the emitter node of the cascode-configured transistors Q7 and Q8, on which the output currents of the three circuit blocks described above may be summed, that is the output currents of the voltage-to-current, fixed gain amplifier (Q1-Q2), of the voltage-to-current, variable gain amplifier (Q3-Q4) and of the variable current generator (Q5-Q6), respectively.

A second function is that of reducing the parasitic capacitance present on the output nodes, which, in absence of the cascode pair Q7-Q8, would be equal to the sum of the parasitic capacitances of three transistors, for example of Q1, Q3 and Q5 on one node and of Q2, Q4 and Q6 on the other node. Moreover, the cascode pair Q7-Q8 eliminates the Miller effect of multiplication of the parasitic capacitance by the gain.

By referring to the identifying symbols of the components of the circuit of the invention, as depicted in Fig. 6, the gain may be calculated as follows:

$$gm_1 = gm_2 = \frac{I0}{Vt}$$

(gm is the transconductance of the relative transistor for small signals; Vt is the "thermal" voltage that is equal to 0.026V at T = 27°C)

$$gm_3 = gm_4 = \frac{I}{Vt}$$

I = Io - DELTAI

$$i_1 = \frac{vs}{2} * \left(\frac{gm1}{1 + gm1 \frac{Re1}{2}} \right) \quad i_2 = - \frac{vs}{2} * \left(\frac{gm1}{1 + gm1 \frac{Re1}{2}} \right)$$

$$i_1 = - \frac{vs}{2} * \left(\frac{gm3}{1 + gm3 \frac{Re2}{2}} \right) \quad i_4 = \frac{vs}{2} * \left(\frac{gm3}{1 + gm3 \frac{Re2}{2}} \right)$$

$i_A = i_1 + i_3$
$i_B = i_2 + i_4$

$$i_A = \frac{v_s}{2} * \left(\frac{gm1}{1 + gm1 \frac{Re1}{2}} - \frac{gm3}{1 + gm3 \frac{Re2}{2}} \right)$$

$$i_B = -\frac{v_s}{2} * \left(\frac{gm1}{1 + gm1 \frac{Re1}{2}} - \frac{gm3}{1 + gm3 \frac{Re2}{2}} \right)$$

$$vout = (i_A - i_B) * R_L$$

$$vout = v_s * \left(\frac{gm1}{1 + gm1 \frac{Re1}{2}} - \frac{gm3}{1 + gm3 \frac{Re2}{2}} \right) * R_L$$

$$G = \frac{vout}{v_s}$$

$$G = 2R_L * \left(\frac{gm1}{2 + gm1 \, Re1} - \frac{gm3}{2 + gm3 \, Re2} \right)$$

$$G = 2R_L * \left(\frac{Io}{2Vt + Io \, Re1} - \frac{I}{2Vt + I \, Re2} \right)$$

$$G = 2R_L * \left(\frac{Io}{2Vt + Io \, Re1} - \frac{Io - DELTAI}{2Vt + (Io-DELTAI)Re2} \right)$$

$$G(DELTAI) = 2R_L * \frac{[Io(Re2 - Re1)(Io - DELTAI) + 2Vt \, DELTAI]}{(2Vt + Io \, Re1)[2Vt + (Io - DELTAI)Re2]}$$

$$GMAX = G(DELTAI = Io) = 2R_L * \left(\frac{Io}{2Vt + Io \, Re1} \right)$$

$$GMIN = G(DELTAI = 0) = 2R_L * \left[\frac{Io^2 (Re2 - Re1)}{(2Vt + Io \, Re1)(2Vt + Io \, Re2)} \right]$$

$$\frac{GMAX}{GMIN} = \frac{(2Vt + Io \, Re2)}{Io (Re2 - Re1)}$$

This last formula permits to easily observe that the range of variation of the gain required by the specification that was reported above (22dB) may be obtained with the following values:

IØ = 200 μA
RE1 = 2000 ohm
RE2 = 2200 ohm

The third functional block of the amplifier of the invention, which is constituted by the variable current generator (Q5-Q6) has also the function of maintaining constant the DC operating point upon the varying of the gain. In order to achieve this result, to the current signals that are summed on the emitter nodes of the cascode stages Q7 and Q8 a complementary current equal to:

Icompl = DELTAI

is added.

The total current that flows through the load resistances RL1 and RL2 in absence of an input signal, once a value for DELTAI has been fixed, is equal to:

$$I_{TOT} = Io + (Io-DELTAI) + (DELTAI) = 2Io$$

and because it does not depend from DELTAI it is independent also from the set gain.

Of course, in order to achieve gain levels that will satisfy the proposed specification of a variable gain amplifier for the type of application considered, the variable gain amplifier, that is the variable gain "cell", object of the present invention, may be followed by a fixed gain amplifier, for example a 10Volt/Volt amplifier.

By simulating the operation of the circuit of the invention with a computer program for evaluating the performance parameters at a supply voltage of 3V, the following results are obtained:
* Typical frequency band > 160 MHz
* Gain variation: from 2.7 to 34 Volt/Volt (22dB)
* Distorsion < 0.7% with an input of 240mVpp
* Output offset: less than +/- 200mV
* Equivalent input noise: < 12nV/sqrt(Hz)
* Absorbed supply current Icc = 1.6mA

As it will be evident to an expert of the field, the circuit object of the present invention may be realized with junction-type, bipolar transistors or in mixed technology by employing for example CMOS transistors for implementing the current generators, or the entire functional circuit of the variable gain cell of the invention may also be realized exclusively with field effect transistors (CMOS) in order to further reduce power consumption.

Claims

1. Variable gain amplifier characterized by comprising
   a first voltage-to-current amplifier having a fixed gain;
   a second voltage-to-current amplifier having a variable gain, functioning in parallel to said first amplifier;
   a gain control and stabilization variable current generator;
   a current-to-voltage converter;
   current output signals produced by said first and second amplifiers and by said variable current generator being summed and the resulting current signal being converted by said converter.

2. A variable gain amplifier according to claim 1, further comprising a summing circuit capable of providing a low impedance node onto which said current output signals are summed.

3. Variable gain amplifier according to claim 2, wherein said summing circuit comprises a pair of cascode configured transistors, functionally connected between the respective output nodes of said first and second amplifiers and of said variable current generator and respective loads, which constitute said current-to-voltage converter.

4. Variable gain amplifier as defined in claim 1, wherein said first fixed gain amplifier is composed of a differential pair of transistors, a degeneration resistance and a pair of bias current generators,
   said second amplifier is composed of a second differential pair of transistors, a degeneration resistance and a pair of variable bias current generators.

5. Variable gain amplifier as defined in claim 1, wherein said transistors are bipolar junction transistors.

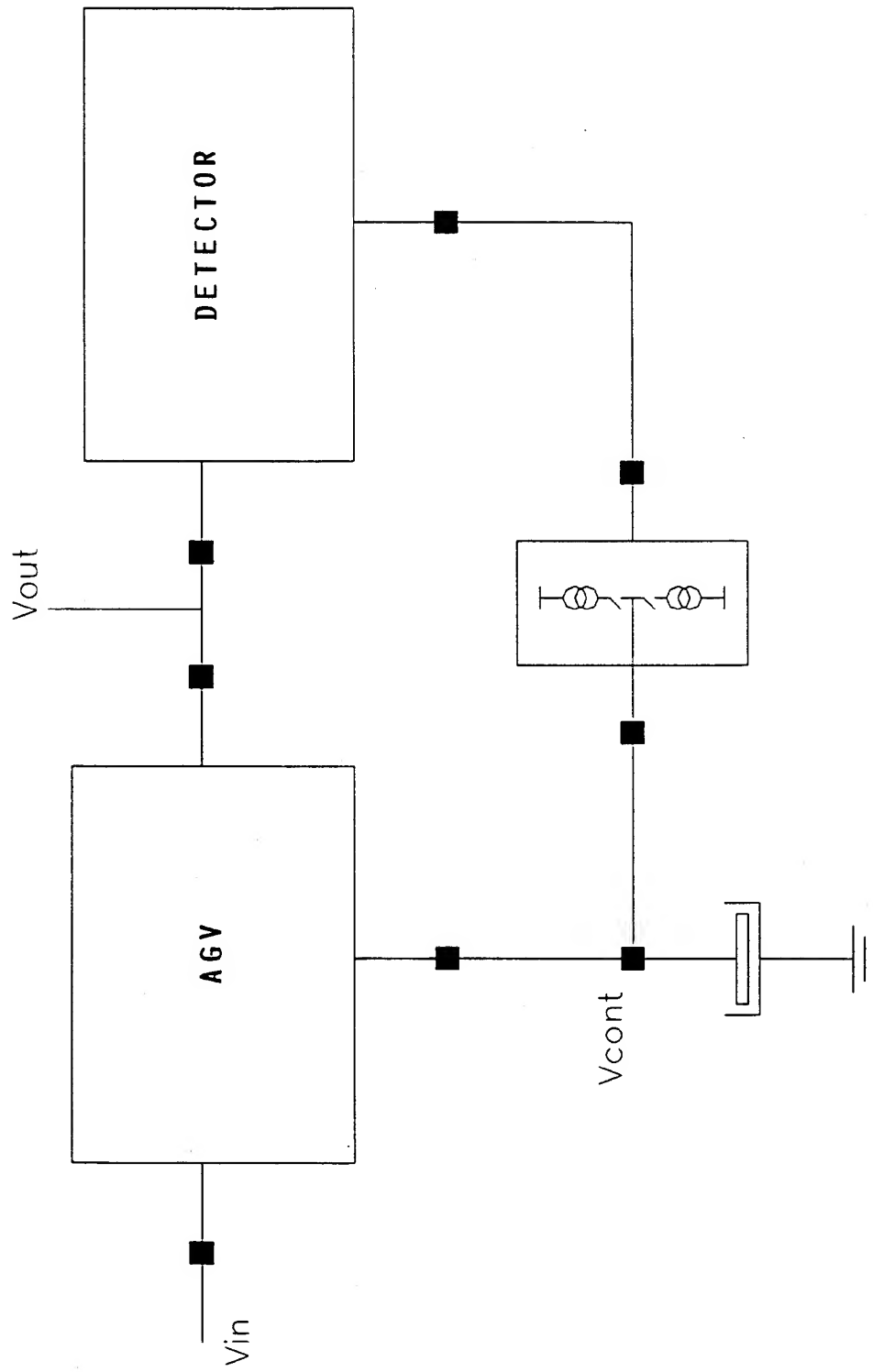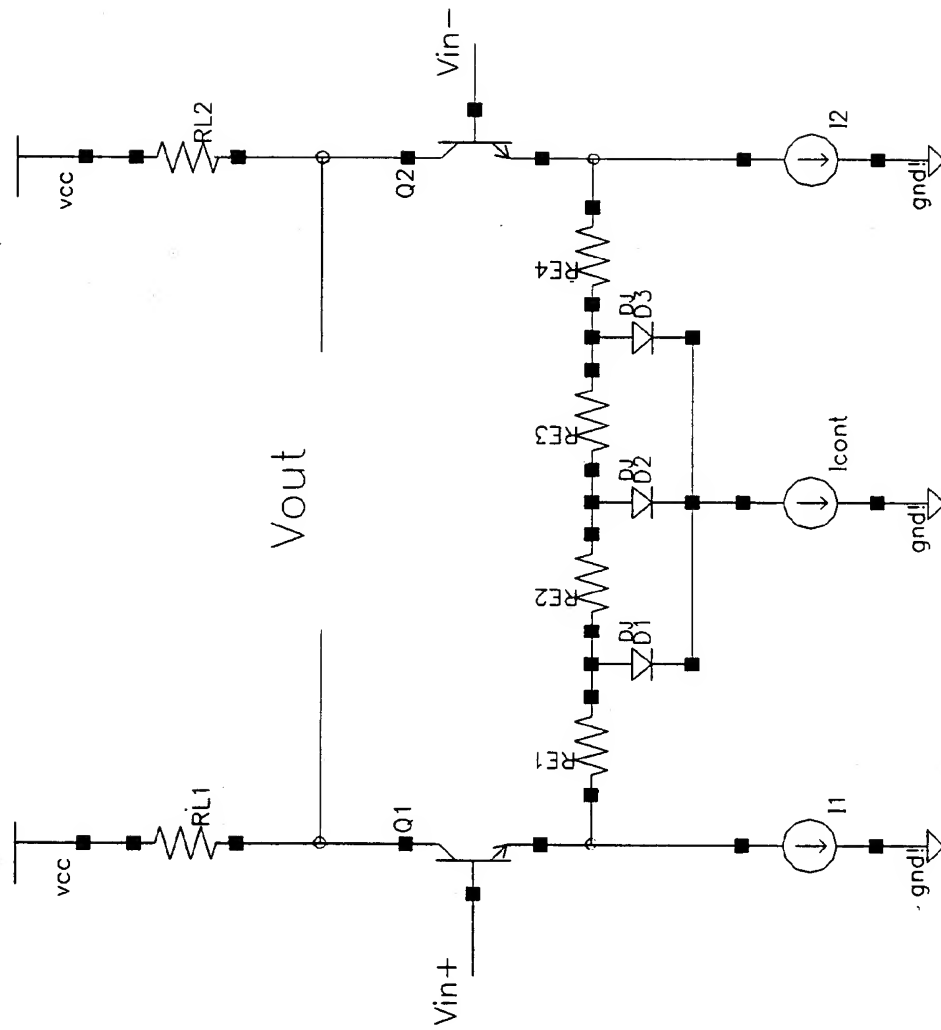6. Variable gain amplifier as defined in claim 1, wherein said transistors are field effect transistors.
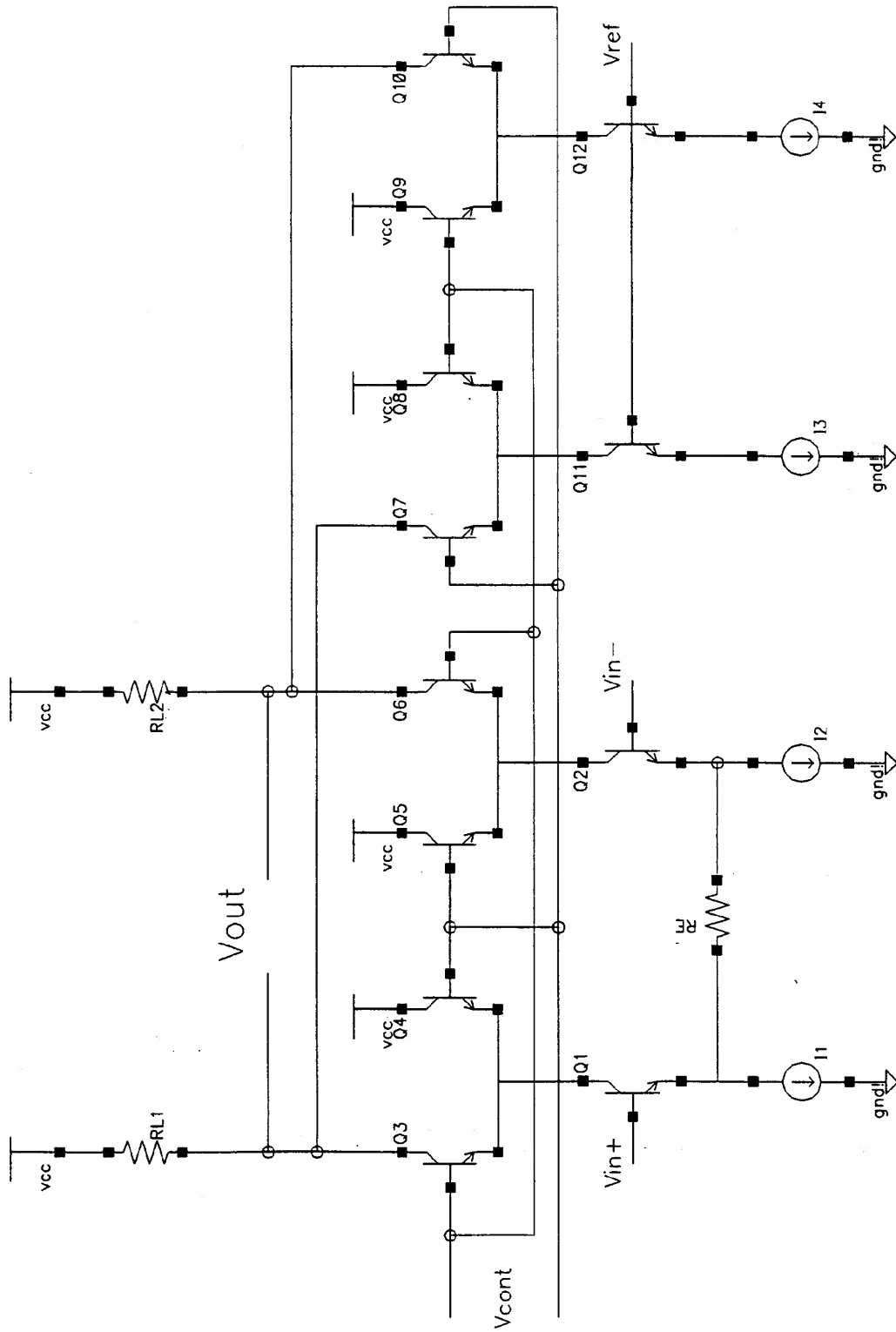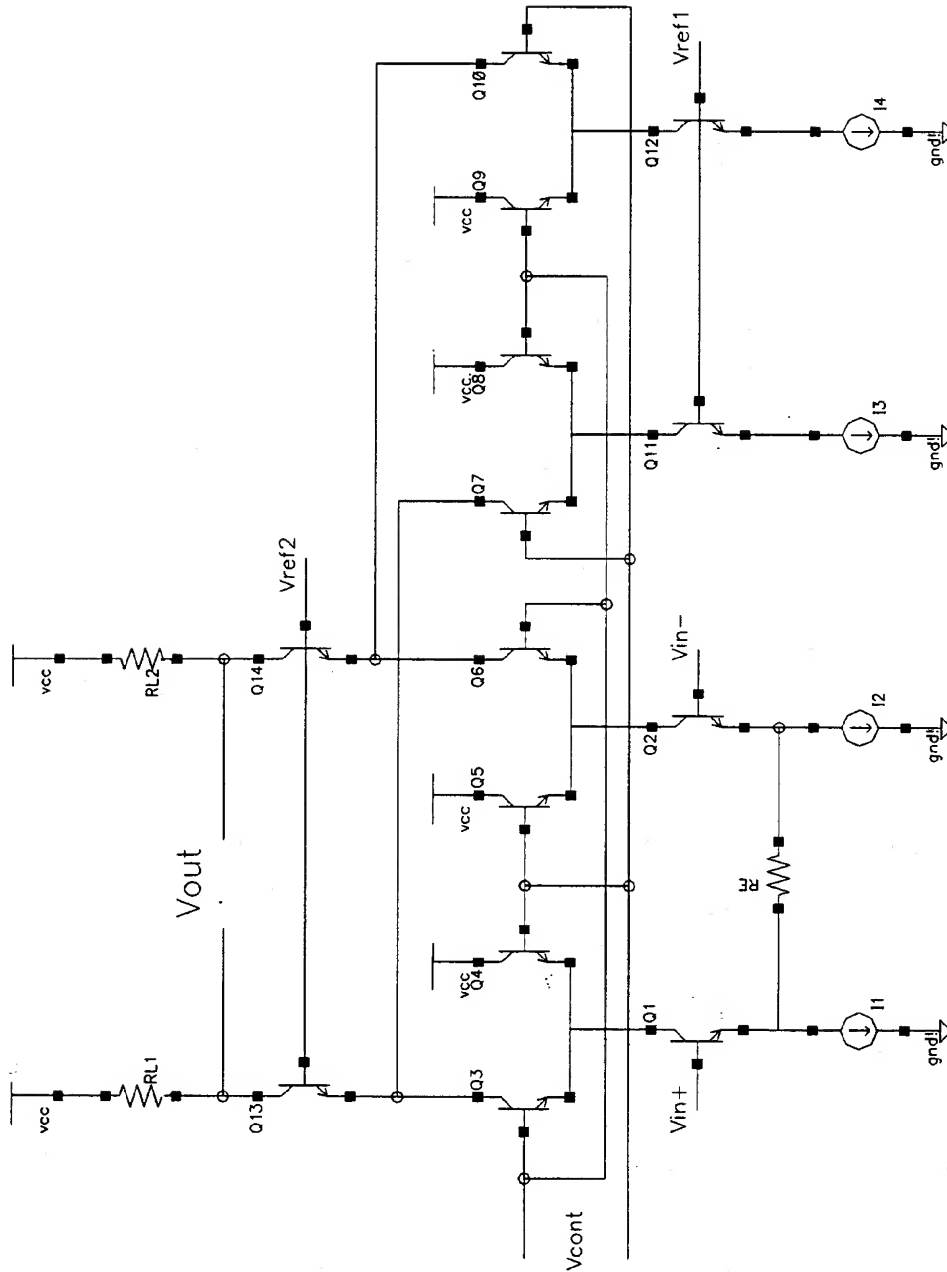
FIG. 1

F I G . 2

F I G. 3

F I G . 4

FIG.5
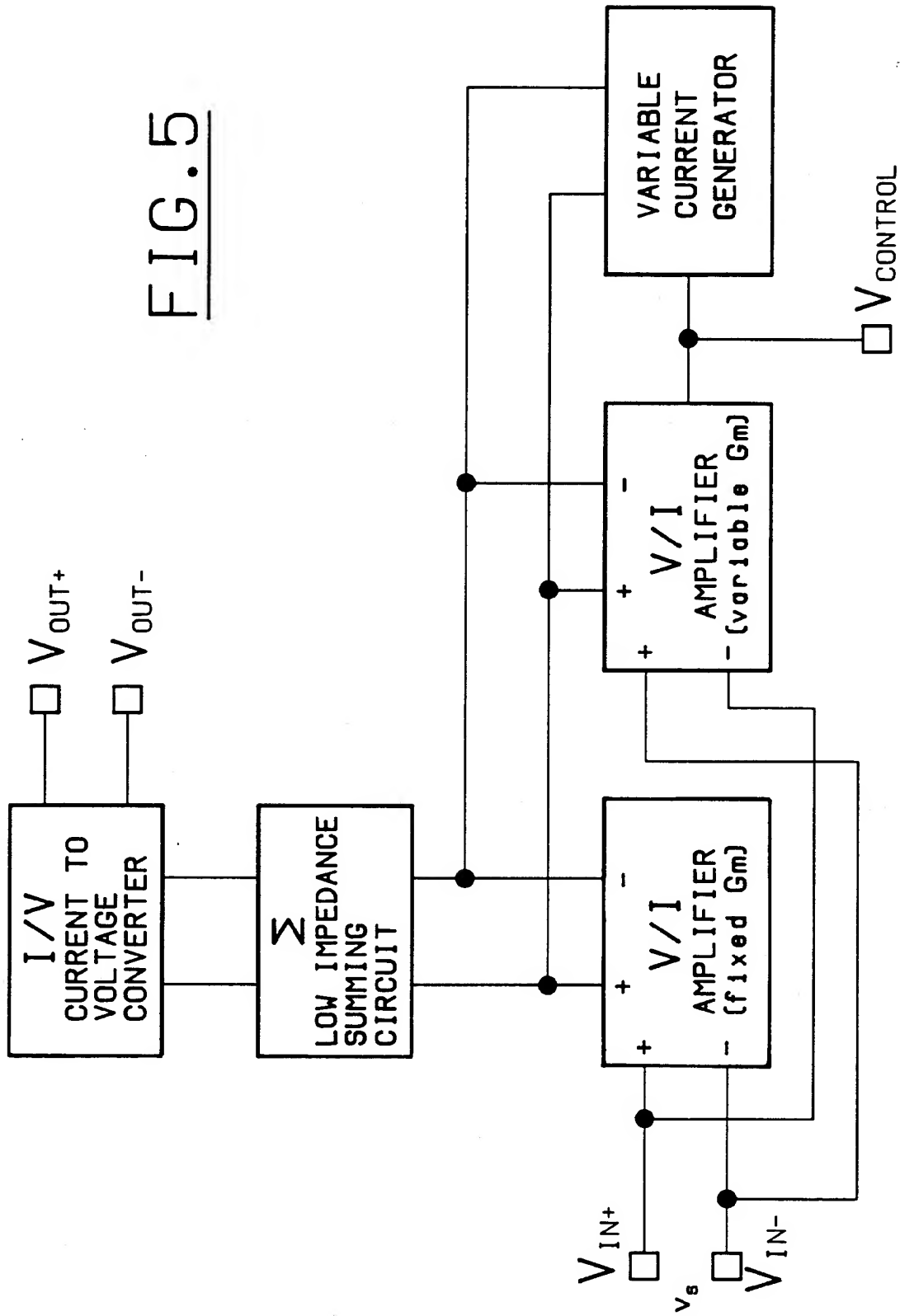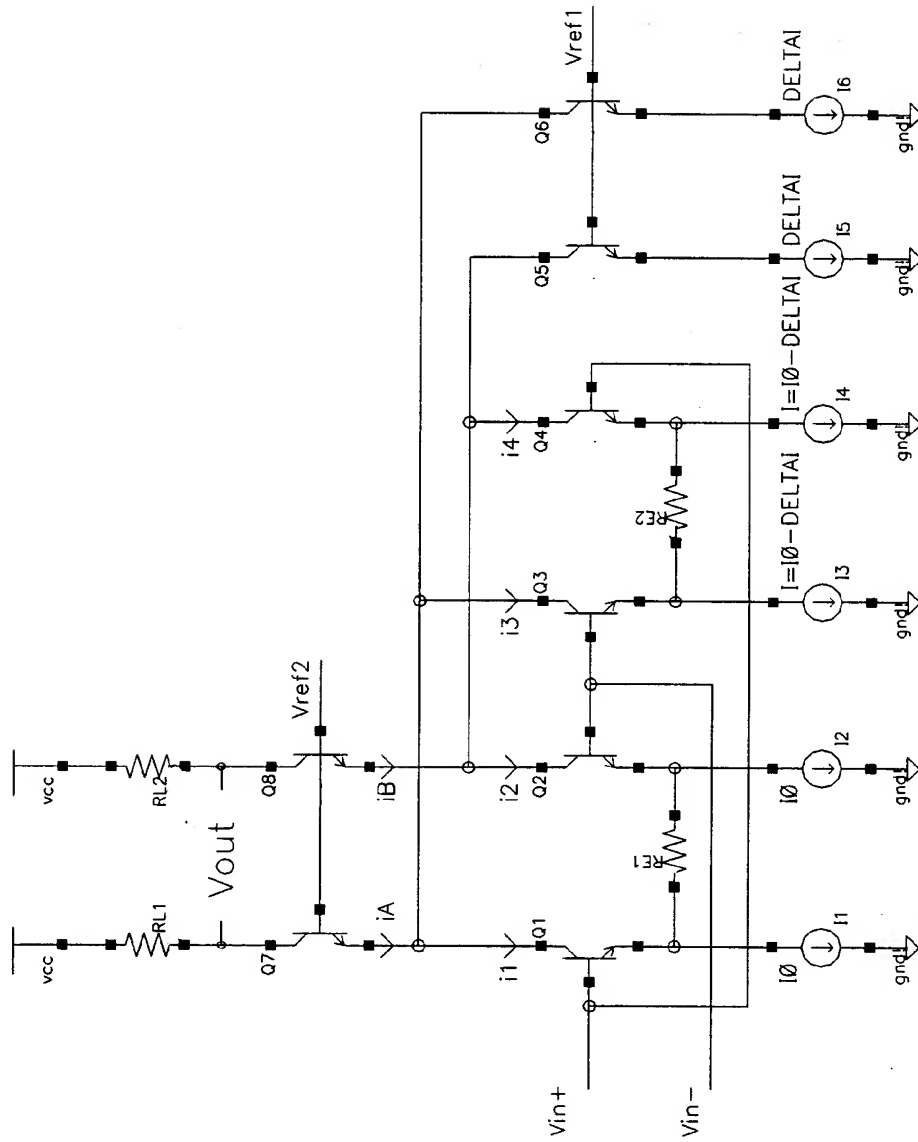
F I G . 6

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	IEEE JOURNAL OF SOLID-STATE CIRCUITS vol. 24, no. 4, August 1989, NEW YORK US pages 951 - 961 TZU-WANG PAN E.A. 'a 50-dB variable gain amplifier using parasitic bipolar transistors in CMOS.' * pg 957-959, chapter 4 : "IV. A variable gain amplifier"* * figure 9 * ---	1	H03G1/00 H03G1/04
A	PATENT ABSTRACTS OF JAPAN vol. 15, no. 169 (P-1196)26 April 1991 & JP-A-30 33 989 (NEC CORP.) 14 February 1991 * abstract * -----	1	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H03G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	07 SEPTEMBER 1993	DECONINCK E.

CATEGORY OF CITED DOCUMENTS

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